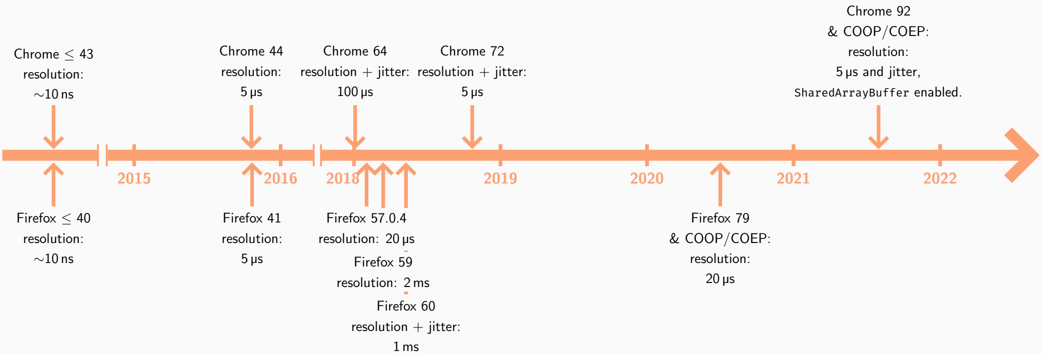
Side Channels in Web Browsers: Applications to Security and Privacy

Thomas Rokicki

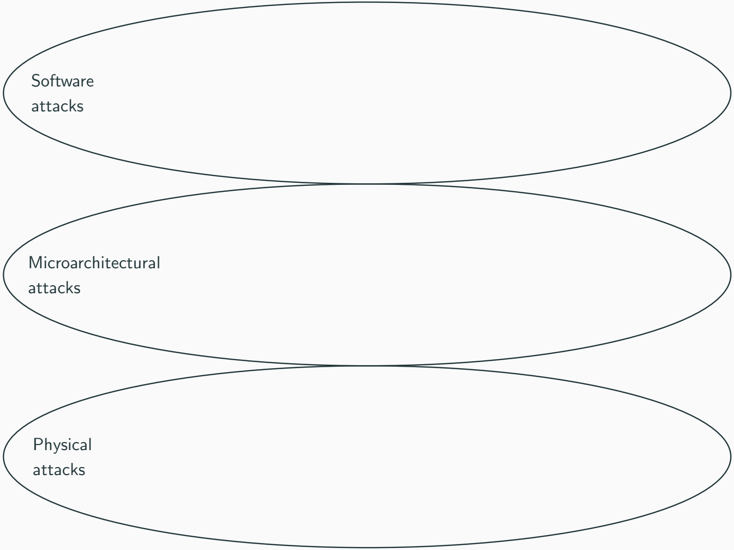
29/11/2022

INSA Rennes, CNRS, IRISA
Supervisors: Clémentine Maurice and Gildas Avoine.

Context


Chrome ≤ 43 resolution: ~10 ns
Chrome 44 resolution: 5 µs
Chrome 64 resolution + jitter: 100 µs
Chrome 72 resolution + jitter: 5 µs
Chrome 92 & COOP/COEP: resolution: 5 µs and jitter, SharedArrayBuffer enabled.
2015
2016
2018
2019
2020
2021
2022
Firefox ≤ 40 resolution: ~10 ns
Firefox 41 resolution: 5 µs
Firefox 57.0.4 resolution: 20 µs
Firefox 59 resolution: 2 ms
Firefox 60 resolution + jitter: 1 ms
Firefox 79 & COOP/COEP: resolution: 20 µs

Context of the contributions



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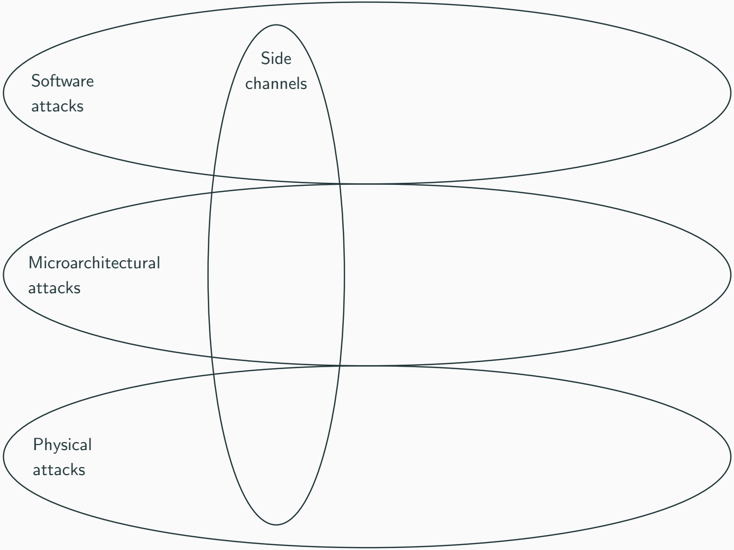

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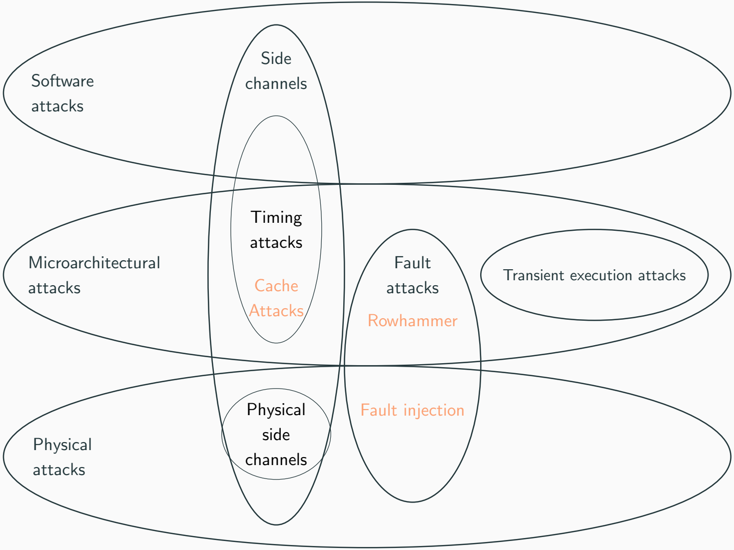

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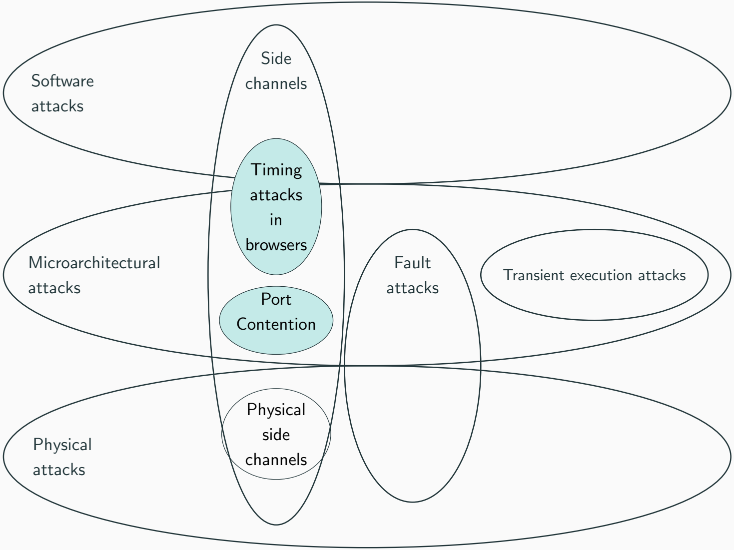

Microarchitectural Side Channels

- Hardware optimizations are designed for performance and not security.
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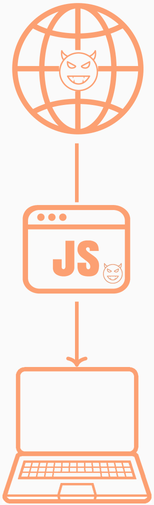
Common prerequisite:
Execute code on shared hardware

Microarchitectural attacks in the browsers: Threat model

- JavaScript or WebAssembly code are client-side languages.



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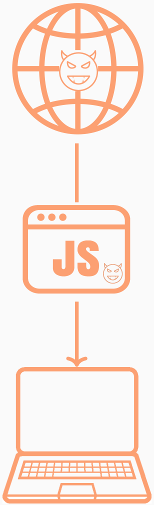

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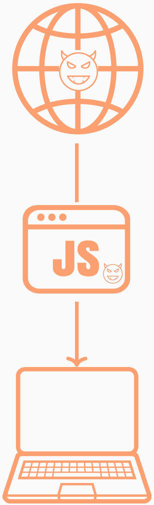


Microarchitectural attacks in the browsers: Common Challenges

- Client-side languages are sandboxed:
  - No native instructions.
  - Oblivious to memory addresses.
  - No access to the filesystem.
- Timers are restricted.
- High-level interpreted languages:
  - JavaScript especially high level.
  - WebAssembly offers more atomic operations.

Research Questions

- With everchanging browsers and microarchitecture, how can we evaluate the threat posed by side channels?
- What side channels can we implement in the browser?
- What information can we extract from these side channels?

Talk Outline

This defense is composed of three major sections:

- **EuroS&P 2021** Systematic analysis of JavaScript timers.
- **AsiaCCS 2022** Port contention in the browser.
- **ESORICS 2022** Port contention without SMT.

In Search of Lost Time: A Survey of JavaScript Timers

Contributions of this Section

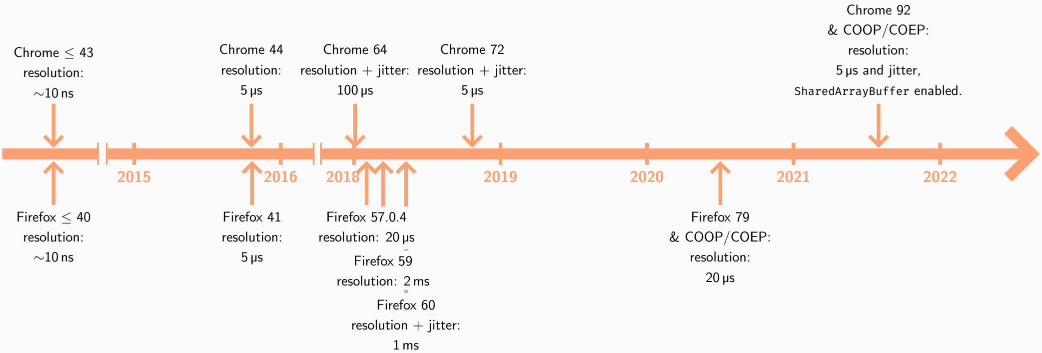
- Classification of browser-based timing attacks.
- Framework to automatically evaluate JavaScript timers.
- Longitudinal study of browsers' timing-based security.

Classification of JavaScript timing attacks

- Hardware-contention-based attacks;
- Transient execution attacks;
- Attacks based on system resources;
- Attacks based on browser resources.

Common prerequisite: Timers.

JavaScript and Timers: A Complicated History



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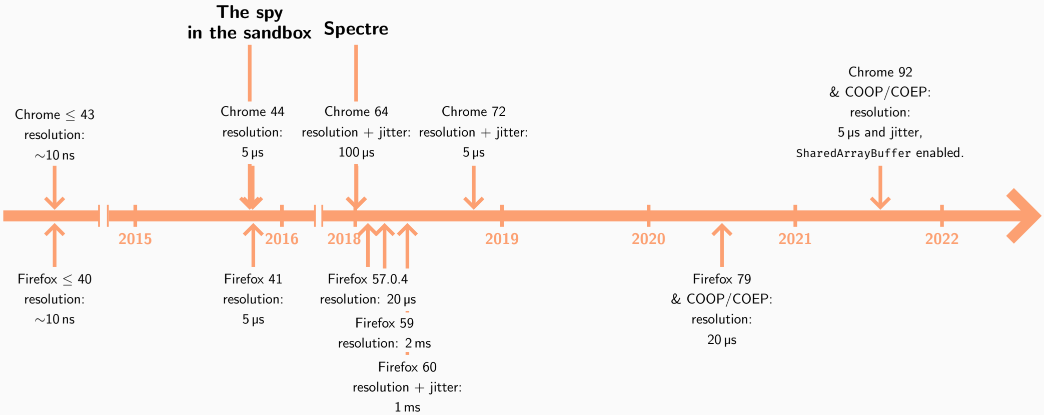

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Built-in timers have a resolution ranging from 5-100 µs.

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  - Grant higher resolution and less jitter.
  - Reactivate `SharedArrayBuffer`.

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What are the security implications of reintroducing high-resolution timers?

Automated Framework

Automated framework to evaluate JavaScript timers using Selenium.

Works on Chrome and Firefox, including past and future versions.

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Works on Chrome and Firefox, including past and future versions.

Our goal is that this analysis can be helpful at this point and in the future.

The code is available here:
https://github.com/thomasrokicki/in-search-of-lost-time

Framework behaviour

For each timer, we evaluate:

Resolution	Smallest operation a timer can measure.
Performance overhead	Time it takes to make the measurement.

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You can find more in-depth details of the experiments and results in the full paper.

Some perspective

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- Create a cache covert channel **800,000** faster.

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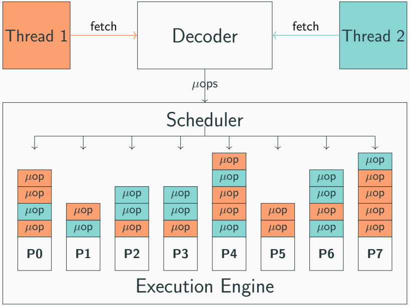
Timing attacks are more of a threat than 4 years ago.

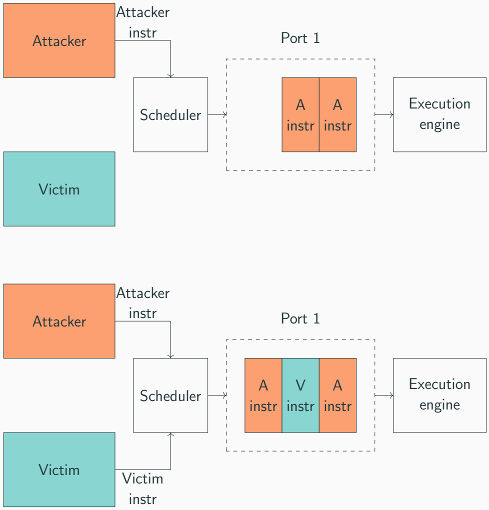
Port Contention Goes Portable

Background: Execution pipeline

- Shared by all threads on the physical core.
- Instructions are decomposed in **micro-operations** (μops).
- The decomposition is **deterministic**.
- μops are dispatched to specialized execution units through **CPU ports**.



Background: Port contention[2]



No Contention All the attacker instructions are executed in a row, **fast execution time**.

Contention Attacker instructions are delayed, **slow execution time**.

[2] Aldaya et al., S&P 2019

C1 - Core control

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Solution: Exploit JavaScript multithreading and work with the scheduler.

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Puts more constraints on core control.

C3 - Port usage of WebAssembly

WebAssembly is a high-level language.

We need to find out the port usage of WebAssembly instructions.

So we built **PC-Detector**

Test the contention of 244 WebAssembly instructions with our knowledge of native port usage.

PC-Detector - Description

Control	The web script runs alone in the browser.
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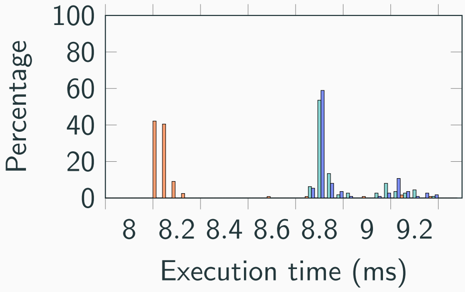
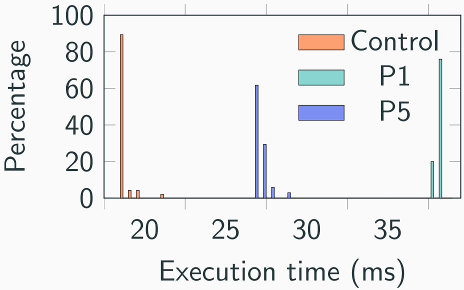


(a) Result for instruction `f64.floor`



(b) Result for instruction `i64.rem_u`

PC-Detector - Results

We tested over 200 different instructions.

- 80 instructions creating contention.
  - Some create more timing difference.
  - `i64.rem_u` seems to cause the most difference in timing.
- Contention on 4 ports: 0, 1, 5, and 6.
  - More threat surface!
  - Ports 2 and 3 have the exact same usage, so execution is always parallelized.

Side-Channel Artificial Example - Description

Generic example of a side channel attack. Web user attacks a native victim and extracts a secret.

Victim

`secret == 0` →

```
POPCNT %r8,%r8
POPCNT %r8,%r8
...
POPCNT %r8,%r8
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```

Contention on Port 1

`secret == 1` →

```
VPBROADCASTD %xmm0, %ymm0
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Contention on Port 5

Monitors port usage

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Contention on Port 5

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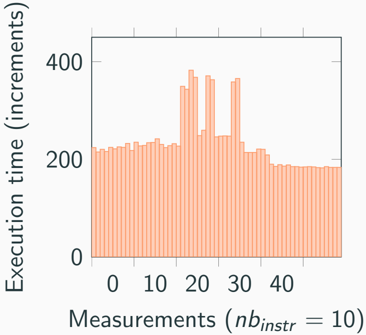

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- Able to detect 1024 native instructions in a single trace.

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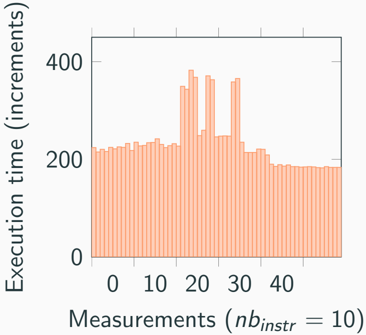

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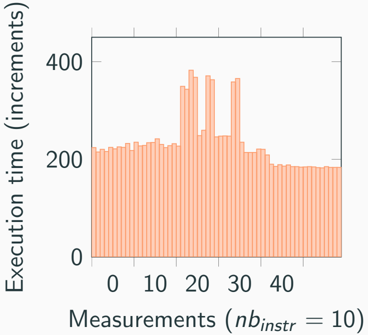

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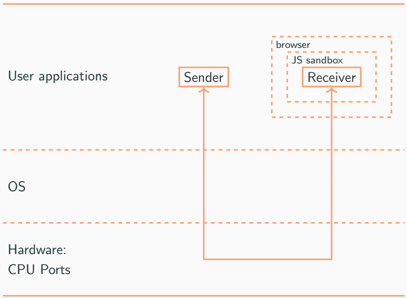
- Timers are the main bottleneck.

Covert Channel

Composed of two components:

- **Native:** C/x86 sender.
- **Web:** JavaScript/WebAssembly receiver.



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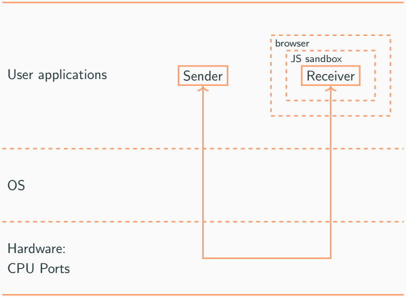
Applications:

- Exchanging cookies/tracking information.
- Extracting native data.



Covert Channel - Physical layer

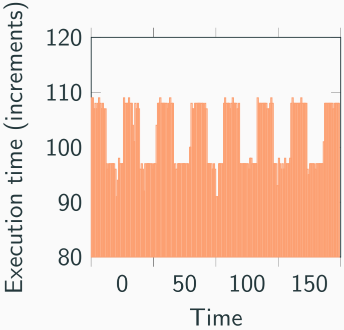


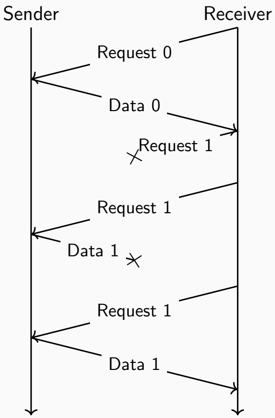
Figure 4: Transmitted square signal

- Sending a 1-bit by creating contention on Port 1
- Receiving bits by measuring execution times of Port 1 instructions
- Fixed bit duration of t_{bit}

Covert Channel - Data-Link layer

Data is separated in frames:

- Sequence number to handle synchronization
- Error-detecting code for bit insertion/deletion



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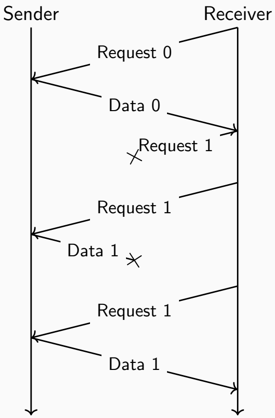

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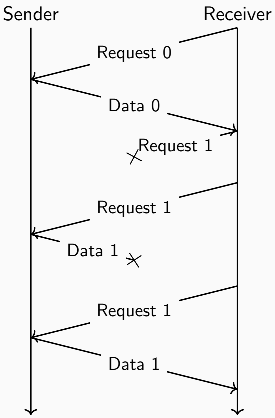
Frame starts are detected using a density clustering algorithm.



Covert Channel - Evaluation

We found $t_{bit} = 1\,\text{ms}$ to be best.

On a quiet system, we obtain the following results:

- 200 bit/s of effective data (Best bandwidth for a web-based covert channel!)
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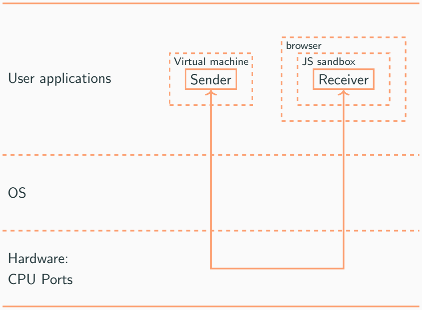
Due to the same-core nature of port contention.

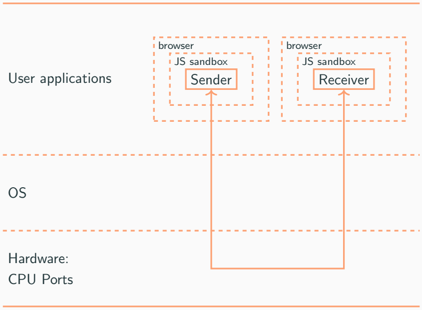
More Covert Channels

VM-to-host



80 bit/s bandwidth.

Cross-browser



200 bit/s bandwidth, across browsers!

Perspective on Web Port Contention

- First implementation of port contention in the browser.
- Fastest covert channel existing in the browser.
- High spatial resolution.
- Breaks the isolation of browser: cross-origin communication is possible, even through virtualized environments.

Sequential Port Contention

Port Contention and SMT

Port contention attacks rely on the attacker and victim sharing a hardware component. They are highly dependent on SMT.

Countermeasures to SMT attacks are starting to appear:

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Can we create port contention without SMT?

Sequential Port Contention

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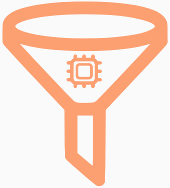

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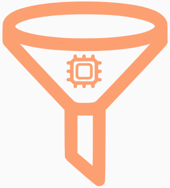

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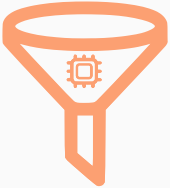
Creates contention on ports and exploits it without SMT.



Port Contention Without SMT - Concept

(a) Grouped

(b) Interleaved

- Both experiments have the same number of instructions.
- Will they have a similar execution time?

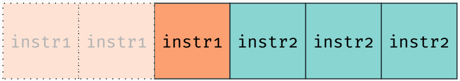
Port Contention Without SMT - Concept

Cycle 0

Port Contention Without SMT - Concept

Cycle 1

Port Contention Without SMT - Concept



Cycle 2

Port Contention Without SMT - Concept

Cycle 3

Port Contention Without SMT - Concept

Cycle 4

Port Contention Without SMT - Concept

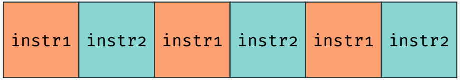
Cycle 5

Execution is never parallelized

Port Contention Without SMT - Concept

Same ports:

Different ports:



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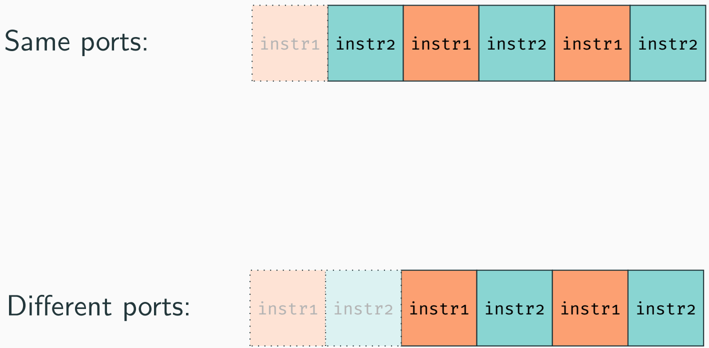

Cycle 1

Port Contention Without SMT - Concept

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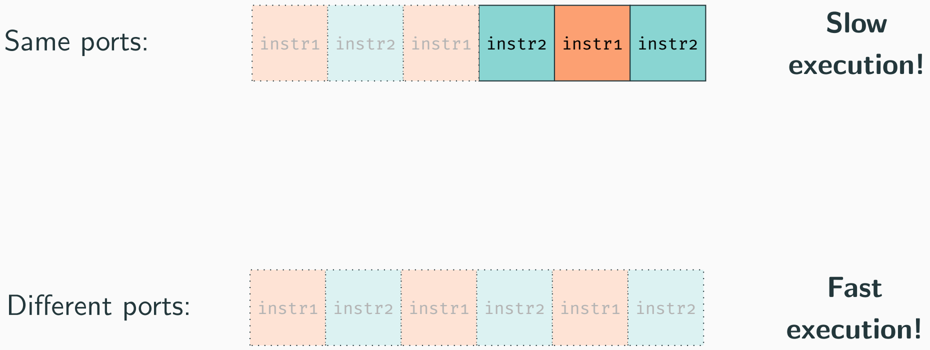
Cycle 2

Port Contention Without SMT - Concept



Cycle 3

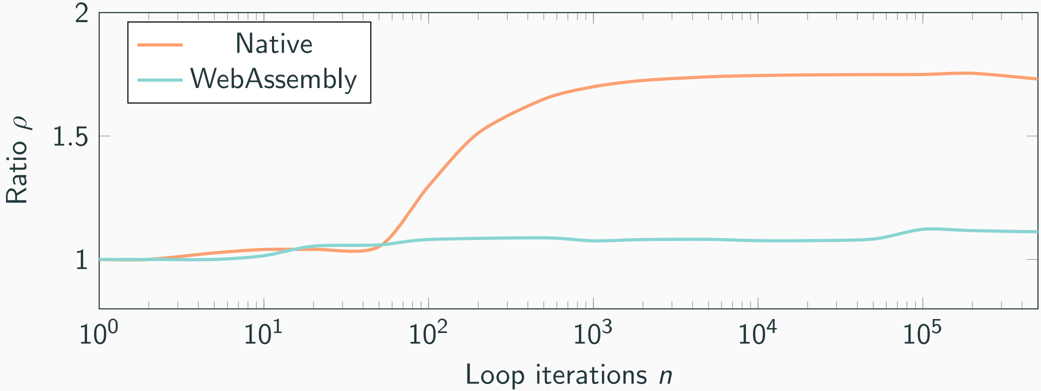


Figure 6: $\rho_{grouped\,/\,interleaved}$.

Application to Fingerprinting - Idea

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- Consolidate software attributes for fingerprinting.

Application to Fingerprinting - Framework

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- Exhibit different contention on different generations;
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We extended **PC-detector** to test 458 pairs of instructions for distinguishers, and found **30**.

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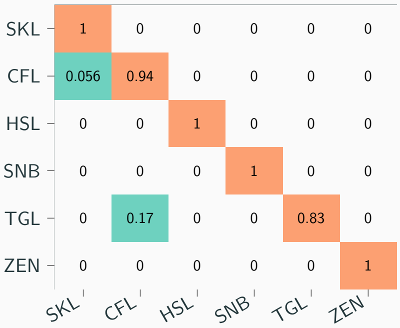
- Once we have these distinguishers, we create **generation fingerprints**, *i.e.*, the behavior of the distinguishers for a given generation.
- We use it to train a k-NN model to classify unknown CPUs.
- We created a website to get these fingerprints: `https://fp-cpu-gen.github.io/fp-cpu-gen` Feel free to try and send us results!

Application to Fingerprinting - Results



- Evaluation on **50** different CPUs, spanning **13 generations**.
- Includes Intel CPUs and AMD.
- **92%** accuracy.
- Highly stable and resistant to noise.

Perspective on Sequential Port Contention

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- Maybe other SMT attacks can be leveraged with instruction-level parallelism?

Conclusion and Future Work

Future Work

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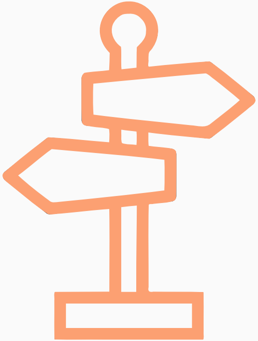
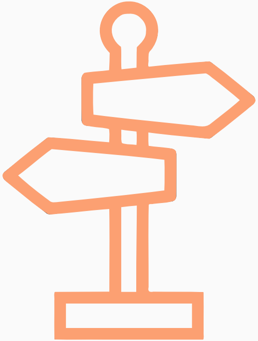


Future Work

- We have many new side channels to discover.
  - Exploit already existing native side channels.
  - Change the attack paradigm to discover new threats.



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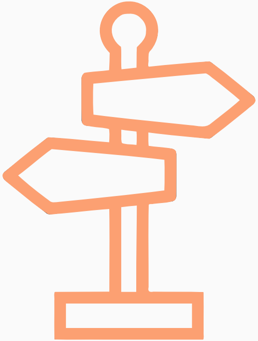

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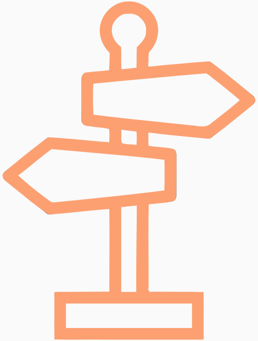

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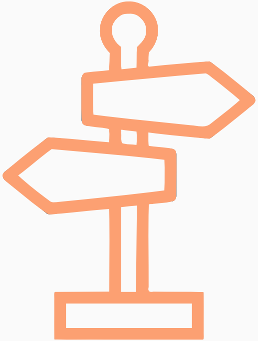

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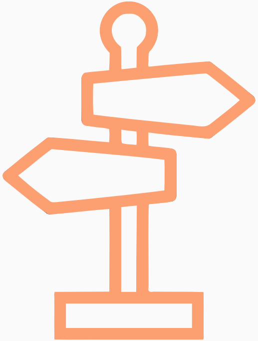

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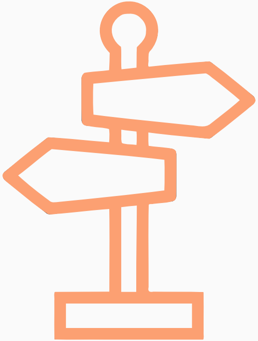

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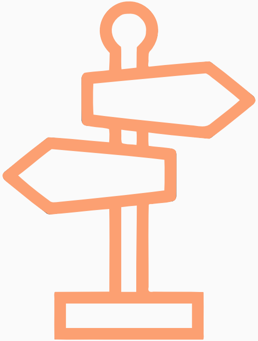
- Hardware browser fingerprinting is promising.
  - As a complement to software fingerprinting.
  - Exploiting imperfection can lead to unique fingerprints.



Contributions

ESORICS 2022 Port Contention Without SMT.
Thomas Rokicki, Clémentine Maurice, Michael Schwarz.

AsiaCCS 2022 Port Contention Goes Portable.
Thomas Rokicki, Clémentine Maurice, Marina Botvinnik, Yossi Oren.

EuroS&P 2021 In Search Of Lost Time.
Thomas Rokicki, Clémentine Maurice, Pierre Laperdrix.

Thank you for your attention!